Scholar **All articles** - Recent articles Results **1** - **10** of about **5,310** for **instruction** (**sub-bundle** **OR** s

Large **parallel** computers
J Schwartz - Journal of the ACM (JACM), 1966 - portal.acm.org
... from a larger group, causing the processors in the **subgroup** to execute ... This can be effectively accomplished by an **instruction** which ... LARGE **PARALLEL** COMPUTERS 29 ...
Cited by 18 - Related articles - Web Search - All 2 versions

... in a multiple **instruction** stream multiprocessor where any of the **parallel** processors is scheduled ...
R Gupta, MA Epstein - US Patent 5,127,092, 1992 - Google Patents
... to processors P1-P4, or a **sub-group** of them involved in branching 30 **parallel instructions**, with the ... processor between such units and **execution** means 12 ...
Cited by 14 - Related articles - Web Search - All 2 versions

Computer architecture capable of concurrent issuance and **execution** of general purpose multiple ...
RW Horst - US Patent 5,752,064, 1998 - Google Patents
... 1013-1022. Tjaden et al.. "Detection and **Parallel Execution** of Indepen- dent **Instructions**," IEEE Transactions on Computers, vol. C-19, No. 10, Oct. 1970. pp. ...
Cited by 8 - Related articles - Web Search - All 4 versions

Integrating synchronous and asynchronous paradigms: the Fork95parallel programming language- ▶psu.edu [PDF]
CW Kessler, H Seidl - Programming Models for Massively **Parallel** Computers, 1995, 1995 - ieeexplore.ieee.org
... language elements (multi- prefix **instructions**, see below ... Now, each **subgroup** continues on exe- cuting ... the processors within each **sub- group** work synchronously ...
Cited by 22 - Related articles - Web Search - Library Search - All 11 versions

[PDF] ▶Fork95 Language and Compiler for the SB-PRAM
CW Keler, H Seidl - Proc. 5th Workshop on Compilers for **Parallel** Computers - Citeseer
... branch of a recursive procedure (like **parallel** depth{rst ... shared memory fraction of each **subgroup** has reached ... **instruction**, and waits until it sees a zero in the ...
Cited by 17 - Related articles - View as HTML - Web Search - All 4 versions

The Fork95 **parallel** programming language: design, implementation, application
CW Keßler, H Seidl - International Journal of **Parallel** Programming, 1997 - Springer
... of control flow and execute the same **instruction** at the ... first iteration of the loop form a **subgroup** g' and ... As an illustration, consider the data **parallel** loop ...
Cited by 18 - Related articles - Web Search - BL Direct - All 4 versions

[PDF] ▶The Fork95 **parallel** programming language: Design, implementation, application
CW Keler, H Seidl - International Journal of **Parallel** Programming, 1996 - Citeseer
... are better language elements (multiprex **instructions**, see subsection ... by the user execute the startup code in **parallel**. ... within each active **subgroup**, the current ...
Cited by 14 - Related articles - View as HTML - Web Search - All 4 versions

A new **parallel** architecture for sparse matrix computation based on finite projective geometries
N Karmarkar - Proceedings of the 1991 ACM/IEEE conference on ..., 1991 - portal.acm.org

... Furthermore the **instruction** set should have a structure ... in solving many difficult problems in **parallel** system design ... to applications that involve **execution** of a ...
Cited by 7 - Related articles - Web Search - All 2 versions

Artificial neural networks on massively **parallel** computer hardware- ▶tu-clausthal.de [PDF]
U Seiffert - Neurocomputing, 2004 - Elsevier
... standard computer languages with information distribution **instructions**. ... Since real **parallel** computers and homogeneous clusters are a **subgroup** of heterogeneous ...
Cited by 32 - Related articles - Web Search - All 14 versions

ForkLight: A control-synchronous **parallel** programming language- ▶psu.edu [PDF]
C Kebler, H Seidl - Proc. High-Performance Computing and Networking, 1999 - Springer
... fetch_add and atomic update **instructions** like atomic_add, which are ... objects can be allocated locally to the **sub- group**. Now, each **subgroup** #i executes < s tint ...
Cited by 3 - Related articles - Web Search - Library Search - BL Direct - All 6 versions

Key authors: **H Seidl - C Keßler - C Keler - J Schwartz - U Seiffert**

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instruction (sub-bundle OR sub-grou Search

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(k)-Instructions-at-a-time pipelined processor for **parallel execution** of inherently sequential ...
HT Hao, H Ling, HE Sachar, J Weiss, YJ Yamour - US Patent 4,594,655, 1986 - Google Patents
... a com- puter architecture with a **group** of differing **...** There is no **parallel execution** of inherently serial **instructions**. **...** for fetching the next 35 **instruction** at a **...**
Cited by 71 - Related articles - Web Search - All 3 versions

... issuing instructions for **parallel execution** subsequent to branch into a **group** of member instructions ...
S Vassiliadis, B Blaner, TL Jeremiah - US Patent 5,303,356, 1994 - Google Patents
... 12, 1994 [54] SYSTEM FOR ISSUING **INSTRUCTIONS** FOR **PARALLEL EXECUTION** SUBSEQUENT TO BRANCH INTO A **GROUP** OF MEMBER **INSTRUCTIONS** WITH COMPOUNDABILITY IN DICTATION **...**
Cited by 19 - Related articles - Web Search - All 2 versions

[PDF] ▶ Introducing the IA-64 architecture
J Huck, D Morris, J Ross, A Knies, H Mulder, R ... - IEEE micro, 2000 - rose-hulman.edu
... (b) Figure 2. IA-64 **bundle** (a) and **...** IA-64 realizes **parallel execution** semantics in the form of **...** groups so that all **instructions** in an **instruction group** can be **...**
Cited by 115 - Related articles - View as HTML - Web Search - BL Direct - All 57 versions

Available **instruction**-level parallelism for superscalar and superpipelined machines- ▶ psu.edu [PDF]
NP Jouppi, DW Wall - Proceedings of the third international conference on ..., 1989 - portal.acm.org
... **instruction** class A **group** of **instructions** all **...** that had only moderate **instruction**-level parallelism. **...** diagram readability only) and **parallel execution** of vector **...**
Cited by 332 - Related articles - Web Search - Library Search - All 11 versions

Hierarchical priority branch handling for **parallel execution** in a **parallel** processor
RP Colwell, JO'Donnell, DB Papworth, PK Rodman - US Patent 4,833,599, 1989 - Google Patents
... neousiy and independently determining, during the **The** invention relates generally to **parallel** data pro- **parallel execution**, a target **instruction** address for **...**
Cited by 50 - Related articles - Web Search - All 3 versions

The IA-64 architecture at work
C Dulong - Computer, 1998 - ieeexplore.ieee.org
... shows the IA-64 **instruction bundle**, which contains **...** a means of expressing explicit **instruction** depen- dencies **...** the compiler to flexibly **group** several independent **...**
Cited by 100 - Related articles - Web Search - BL Direct - All 7 versions

An abstract machine for restricted AND-**parallel execution** of logic programs
MV Hermenegildo - Third International Conference on Logic Programming, 1986 - Springer
... most proposed **parallel** logic programming **execution** models lack **...** This paper presents a **parallel** abstract machine which **...** A suitable **instruction** set, which can be **...**
Cited by 101 - Related articles - Web Search - All 4 versions

Instruction-level **parallel** processing: history, overview, and perspective- ▶ umich.edu [PDF]
BR Rau, JA Fisher - The Journal of Supercomputing, 1993 - Springer
... 1989]. As a **group** these companies were able to demonstrate that it was possible to build **...** The end result of **instruction**-level **parallel execution** is that **...**

Cited by 364 - Related articles - Web Search - Library Search - All 17 versions

Data processing apparatus for highly **parallel execution** of stored programs
JB Dennis, DP Misunas - US Patent 4,153,932, 1979 - Google Patents
... Rodriguez, JE A Graph Model for **Parallel** Com- putation ... and filtering, in which a **group** programming language ... is data-driven; that is, each **instruction** is enabled ...
Cited by 56 - Related articles - Web Search - All 4 versions

Advanced Performance Features of the 64-bit PA-8000- ▶ed.ac.uk [PS]
D Hunt - Compcon'95.'Technologies for the Information Superhighway', ..., 1995 - ieeexplore.ieee.org
... the more likely it is that the **instruction group** will contain **instructions** which de ... in order to find opportunities for **parallel execution**, rather thank ...
Cited by 135 - Related articles - Web Search - BL Direct - All 6 versions

Key authors: **J Fisher - N Jouppi - J Dennis - H Sharangpani - T Conte**

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instruction (bundle OR group) parall Search

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(details)

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... issuing instructions for **parallel execution** subsequent to branch into a **group** of member instructions ...
S Vassiliadis, E Blaner, TL Jeremiah - US Patent 5,303,356, 1994 - Google Patents
... ivrvirvj-ri™ BRANCH INTO A **GROUP** OF MEMBER ... digital computers and digital DICTATION **TAG** data processors ... This application claims **priority** and USA continua- 10 ...
Cited by 19 - Related articles - Web Search - All 2 versions

Hierarchical **priority** branch handling for **parallel execution** in a **parallel** processor
RP Colwell, JO'Donnell, DB Papworth, PK Rodman - US Patent 4,833,599, 1989 - Google Patents
... 1 **TAG** BUSSES Page 3. ... 4,833,599 1 2 tentative **order** of **execution** for the branch instructions ... HIERARCHICAL **PRIORITY** BRANCH The method further features the steps of ...
Cited by 50 - Related articles - Web Search - All 3 versions

The mentat run-time system: Support for medium grain **parallel** computation
A Grimshaw - Distributed Memory Computing Conference, 1990., Proceedings ..., 1990 - ieeexplore.ieee.org
... system delivers the message to the **token** match- ing ... and are evaluated in the **order** of their **priority**. ... Mentat object invoked, the computation **tag** that uniquely ...
Cited by 34 - Related articles - Web Search - Library Search

[CITATION] AND **parallel** Prolog with divided assertion set
H Nakagawa - International Symposium on Logic Programming: Proceedings, 1984 - IEEE Computer Society Press
Cited by 6 - Related articles - Web Search

Issue logic for a 600-mhz out-of-**order execution** microprocessor- ▶ seu.edu.cn [PDF]
JA Farrell, TC Fischer - IEEE Journal of Solid-State Circuits, 1998 - ieeexplore.ieee.org
... sum all five invalid bits in each **group**, similar to ... The center box adds by shifting a **token** left one bit ... issue each cycle with a novel cascaded **priority** encoder ...
Cited by 74 - Related articles - Web Search - BL Direct - All 7 versions

Mul-T: A high-performance **parallel** Lisp
DA Kranz, RH Halstead Jr, E Mohr - Proceedings of the ACM SIGPLAN 1989 Conference on ..., 1989 - portal.acm.org
... task it searches for an- other according to the following **priority order**: ... **order** byte of a word as the **tag** field is ... a **group**, no other tasks in the **group** wil1 run ...
Cited by 139 - Related articles - Web Search - All 3 versions

[PDF] ▶ Shared data spaces for distributed computing and parallelism in scientific visualization systems
M Grave - CWI Quarterly, 1994 - Citeseer
... Note that the use of testag and **tag**-range is ... to give locally available pieces in **priority**, in **order** ... All other members of the Graphics **Group** also contribute to ...
Cited by 6 - Related articles - View as HTML - Web Search - All 3 versions

Itanium 2 processor microarchitecture- ▶ polimi.it [PDF]

C McNairy, D Soltis - IEEE Micro, 2003 - ieeexplore.ieee.org
... The **tag** in way 2 matches the match line, so way 2 is ... or the instruction buffer is empty, a **bundle** can bypass ... The instruction in an issue **group** is determined at ...
Cited by 114 - Related articles - Web Search - BL Direct - All 40 versions

... data collision on data bus for out-of-**order** memory accesses with access **execution** time based in ...
H Stracovsky, P Szabelski - US Patent 6,587,894, 2003 - Google Patents
... 1E.1 **Group Priority** Selector Register 154 76543210 0 0 0 1 ... LJ1 L|2 L3...LO - Livelock for **priority** "00" to ... r Page Write ADD, 100 3 \ state of **tag** after request ...
Cited by 4 - Related articles - Web Search - All 2 versions

Grid'BnB: A **Parallel** Branch and Bound Framework for Grids- ▶ inria.fr [PDF]
D Caromel, A di Costanzo, L Baduel, S Matsuoka - Lecture Notes in Computer Science, 2007 - Springer
... **order** tasks have been sent to the master, and **priority** explores in **priority** branches that ... **Group** of Workers with Node **Tag** 0-1 **Group** of Workers with NodeTag 0-2 ...
Cited by 3 - Related articles - Web Search - BL Direct - All 3 versions

Key authors: **R Halstead - J Farrell - D Kranz - C McNairy - F Noreils**

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